

Appendix – 1

Sr. No.	Course Name	Code		0			Teaching Scheme		0		0		0		0		0		0		0		0		0		0		0		Credit	Examina	Total
			L	T	P		Theory	Tutorial	Practical																								
1	DIGITAL VLSI DESIGN(NEW)	EC 609	3	0	0	3	100			100																							
2	MOS DEVICES AND TECHNOLOGY(NEW)	EC 611	3	0	0	3	100			100																							
3	EMBEDDED SYSTEMS(NEW)	EC 613	3	0	0	3	100			100																							
4	VLSI LAB - I(NEW)	EC 615	0	0	8	4			100	100																							
5	Elective I	EC 6XX	3	0	0	3	100			100																							
6	Elective II	EC 6XX	3	0	0	3	100			100																							
Tota	1		15	0	8	19	500		100	600																							

LIS	Γ OF SUBJECTS FOR ELECTIVE	I & II:
(01)	RF Circuits & Systems	EC601
(02)	Advance DSP	EC605
(03)	Information Theory & Coding	EC619
(04)	VLSI Technology	EC617
(05)	Hardware Description Language	EC623
(06)	Device Modeling & Simulation	EC625
(07)	Probability and Random Processes	EC629



Appendix 2

M. Tech. I (EC) [VLSI/CS] Semester I	L	T	P	C	
EC609:DIGITAL VLSI DESIGN(NEW)	3	0	0	3	
INTRODUCTION TO VLSI DESIGN					(05 Hours)
Historical Perspective, Design Hierarchy, Concepts Of Regularion Styles, VLSI Design Flow, Computer-Aided Design Technology	•	ularit	y An	d Loca	lity, VLSI Design
MOS INVERTER					(06 Hours)
Static Characteristics: Introduction, Resistive Load Inverter, In Inverter, Switching Characteristics And Interconnect Effects, I Delay Times, Inverter Design With Delal Constraints, Estimation Interconnect Delay, Switching Power Dissipation Of CMOS In	ntroduc on Of I	tion,	Defi	nitions	And Calculations Of
CIRCUIT CHARACTERIZATION AND PERFORMANC	E EST	IMA'	ΓΙΟΝ	1	(06 Hours)
Delay Estimation, Logical Efforts And Transistor Sizing, Power Reliability	r Dissi	pation	n, Int	erconn	ect, Design Margin,
COMBINATIONAL AND MOS SEQUENTIAL LOGIC C	IRCUI	TS			(06 Hours)
CMOS Logic Circuits, Complex Logic Circuits, Behavior Of N Clocked Latch And Flip-Flop Circuits, CMOS D-Latch And F					
DYNAMIC LOGIC CIRCUIT					(06 Hours)
Pass Transistor Circuits, Voltage Bootstrapping, Synchronous I High Performance Dynamic CMOS Circuit	Dynami	c Cir	cuit 7	Γechnic	lues, Dynamic And
DIGITAL SUBSYSTEM DESIGN					(13 Hours)
Semiconductor Memory Design, Schmitt Trigger, Multivibrator Adders, Multipliers And Shifters	Circui	t, Dig	gital]	Phase I	Locked Loop,
			(To	tal Co	ntact Time:42 Hours)
BOOKS RECOMMENDED					
1. Kang and Leblebici, "CMOS Digital Integrated Circuits: Ana Edition, 2003	lysis ar	id De	sign"	, Tata	McGraw-Hill, 3rd
2. Baker R. Jacob, Li H. W. & Boyce D. E., "CMOS Circuit De Of India, 2nd Edition, 1998	sign, La	ayout	And	Simula	ation", Prentice-Hall
3. Jan M. Rabey, Anantha Chandrakasan, Borivoje Nikolic, "D 2nd Edition, 3rd Indian Reprint, 2004	igital Iı	ntegra	ited (Circuit'	P, Pearson Education,
4. Weste and Harris, "CMOS VLSI Design: A Circuits and Sys Edition, 2002	tems Pe	erspec	etive"	, Pears	on Education, 3rd
5. Pucknell and Eshraghian: "Basic VLSI Design", Prentice Ha	ll of Inc	dia, 3	rd Ec	lition, 2	2003

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M. Tech. I (EC) [VLSI] Semester I	L	T	P	C	
EC611:MOS DEVICES AND TECHNOLOGY(NEW)	3	0	0	3	
INTRODUCTION TO QUANTUM MECHANICS					(09 Hours)
Principles Of Quantum Mechanics, Schrodinger's Wave Equation, Ap Equation, Electrical Conduction In Solid, Density Of State Function	-				•
PHYSICS OF SEMICONDUCTOR					(12 Hours)
Semiconductor In Equilibrium, Carrier Transport Phenomena, Non E Semiconductor	quili	briun	n Exc	cess C	arries In
PN JUNCTION DIODE					(05 Hours)
PN Junction Current, Small Signal Model, Generation And Recombin	natio	ı Cuı	rent,	Junct	ion Break Down
FUNDAMENTAL OF MOSFET (08 Ho					
Metal Semiconductor And Hetero Junctions, Two Terminal MOS Str Operation, Frequency Limitation	uctui	e, C	V Ch	aracte	ristics, MOSFET
ADVANCE MOS DEVICES					(04 Hours)
FABRICAION OF MOSFET					(04 Hours)
Fabrication Process Flow, CMOS N-Well Process, Layout Design Ru	iles, l	MAS	K La	yout,	Stick Diagram
		(Te	otal (Conta	ct Time: 42 Hours)
BOOKS RECOMMENDED:					
1. Donald Neaman, "Semiconductor Physics and Devices", McGraw H	Iill,T	hird 1	Editi	on,200)7
2. Sze S. M., "Semiconductor Devices, Physics And Technology", Jo	hn W	iley	and S	Son s	2nd Edition,2002
3. Sze S. M., "Physics of Semiconductor Devices", John Willey 2nd F	Editio	n,198	81		
4. Streetman, "Solid State Electronics Device", HI, 2000					
5. Baker R. Jacob, Li H. W. & Boyce D. E., "CMOS Circuit Design, Layout and Simulation", Prentice-Hall Of India, 2nd Ed., 1998					



M. Tech. I (EC) [VLSI/CS] Semester I	\mathbf{L}	T	P	C	
EC613:EMBEDDED SYSTEMS(NEW)	3	0	0	3	
INTRODUCTION TO EMBEDDED SYSTEMS					(04 Hours)
Overview, Categories, Characteristics, Application Areas, Vs SICS Architecture, RTOS Overview of 8 Bit Microco				Systen	n Development,RICS
OVERVIEW OF 8 BIT MICROCONTROLLER					(06 Hours)
Brief Review Of 8 Bit Microcontroller, Programming, CI And Interfacing, High Speed Output, Interrupts, ADC, PV Port		_		•	•
ARM ARCHITECTURE					(13 Hours)
Resisters, Current Program Status Resister, Pipeline, Exce Arm And Thumb Mode Memory Management Unit, Arm Processor Architecture	•	-			
ARM SOFTWARE DEVELOPMENT					(05 Hours)
Arm & Thumb Instruction Set: Data Processing Instruction Program Status Resister Instruction, Loading Constant, Secondary 1988					
'C' Programming ARM					(05 Hours)
Overview Of C Compiler, Basic 'C' Compiler, C Looping Pointer Aliasing, Structure Arrangement, Bit Fields, Unal Point, Inline Function And Inline Assembly	•				
COMMUNICATION INTERFACE					(09 Hours)
RS 232, UART, USB, RS485, Infrared, Ethernet, IEEE80	2.11, Blue	tooth,	SPI, I	2C, CA	N
			(To	tal Co	ntact Time:42 Hours
POOKS DECOMMENDED					
1. Kenneth Ayala J., "8051 Microcontroller: Architecture, Edition, 2006	Programn	ning &	App	lications	s", Thomson, 1st
2. Sloss and System, "ARM System Developer's Guide: I Software", Elsevier, 2004	Designing a	and Op	otimac	y Syste	m
3. Rajkama, "Embedded System Architecture, Programmi	ng and De	sign",	Tata	McGrav	w- Hill,2004
4. Mazidi and Mazidi, Rolin D. McKinlay, "The 8051 Mi Assembly and C", PHI, 3rd Edition, 2004	crocontroll	er and	Emb	edded S	systems using
5. Prasad K. V. K. K., "Embedded / Real-Time Systems:	Concepts,	Design	n And	Progra	mming", Dreamtech

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Press, 2005



M. Tech. I (EC) [VLSI] Semester I	L	T	P	C	
EC615:VLSI LAB - I(NEW)	0	0	8	4	
01. Introduction Of IC Design And IC Layout Software Tool					
02. Realization Of MOS Characterizing					
03. CMOS Inverter VTC & Layout					
04. Introduction Of HDL Software Tool					
05. Implementation Of Array Sub System Using HDL					
06. Device Fabrication Simulation Using TCAD					
07. Realization Of MOS Capacitor And Its Simulation In Various Re	egions	Of O	perat	ion	
08. Analysis Of Scaling Down On MOSFETS					
09. Implementation Of Multiple Gate MOSFETS					
10. 2D/3D Simulation Of Photonic Devices.					
11. Introduction To Embedded Software-Hardware Tool Chain (Comp	olier, D	ebug	ger, S	Simula	ation, Hardware
Kit)					
12. Writing Software (Assembly / C) For ADC / DAC, PWM, GPIO	, Seria	l Port	t, US	B, Int	terrupt RS485
Using 8 Bit Microcontroller & ARM7					



LIST OF SUBJECTS FOR ELECTIVE I & II:

M. Tech. I (EC) [CS/VLSI] Semester I	L	T	P	C	
EC601:RF CIRCUITS & SYSTEMS(NEW)	3	0	0	3	
INTRODUCTION					(02 Hours)
RF Behavior of Passive Components, Chip Components					
TRANSMISSION LINE ANALYSIS					(03 Hours)
Transmission Lines, Equivalent Circuit Representation, Theoretical Plate Transmission Line, General Transmission Line Terminated Lossless Transmission Line, Special Termination Transmission Line, Problems	Equation,	Micro	ostrip	Tran	smission Lines,
SMITH CHART					(03 Hours)
From Reflection Coefficients to Load Impedance, Impedance Parallel and Series Connection, Problems	Transfor	matic	on, A	dmitta	nce Transformation,
SINGLE- AND MULTIPORT NETWORKS					(02 Hours)
Basic Definitions, Interconnecting Networks, Network Proper Definition And Meaning Of S- Parameters, Problems	rties And	App	licati	on,Sc	attering Parameters-
RF FILTERS DESIGN					(06 Hours)
Basic Resonator And Filter Configurations, Special Filter Rea	alizations,	Filte	er Im	pleme	ntation
MATCHING AND BIASING NETWORKS					(04 Hours)
Impedance Matching using Discrete Components, Microstrip Operation & Biasing Networks, Problems solutions	Line Mat	ching	g Net	works	, Amplifier Classes of
POWER DIVIDERS AND DIRECTIONAL COUPLERS					(04 Hours)
The T - Junction Power Divider, The Wilkinson Power Divided Directional Couplers, Problems	er, The Q	uadra	iture	(90°)	Hybrid, Coupled Line
BASIC BLOCKS IN RF SYSTEMS					(03 Hours)
Receiver And transmitter Architectures, Low Noise Amplified Various Mixers	r Design,	Desi	gn A	nd Im	plementation Of
RF OSCILLATORS & SYNTHESIZERS					(07 Hours)
Basic Topologies, VCO And Definition of Phase Noise, Noise Design, Quadrature And Single-Sideband Generators, PLLS, VFrequency Dividers					
DESIGN ISSUES					(04 Hours)
Linearization Techniques, Power Amplifier Design, Integrated	RF Filte	ers			
MMIC					(04 Hours)
Materials, MMIC Growth, Thin Film Formation, Hybrid IC F	ormation				
			(Tota	al Co	ntact Time: 42 Hours

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BOOKS RECOMMENDED:

- 1. Ludwig Reinhold and Bretchko Powel, "RF Circuit Design", Pearson Education, Reprint 2004
- 2. Pozar M. David, "Microwave Engineering", John Wiley & Sons, Inc., 1999
- 3. Liao Samuel, "Microwave Devices And Circuits". Pearson Education, Second Reprint, 2006
- 4. Bhat Bharathi and Koul Shibon, "Stripline-Like Transmission Lines For MIC", New Age International, Reprint

2003

5. Razavi B., "RF Microelectronics", Prentice-Hall PTR,1998

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डिपार्टमेंट ऑफ़ इलेक्ट्रॉनिक्स इंजीनियरिंग

DEPARTMENT OF ELECTRONICS ENGINEERING सरदार वल्लभभाई नेशनल इंस्टिट्यूट ऑफ़ टेक्नोलॉजी, सूरत SARDAR VALLABHBHAI NATIONAL INSTITUTE OF TECHNOLOGY, SURAT

				_				
M. Tech. I (EC) [CS/VLSI] Semester I	L	T	P	C				
EC605:ADVANCE DSP(NEW)	3	0	0	3				
REVIEW OF DISCRETE SIGNAL REPRESENTATION A	(06 Hours)							
TIME AND FREQUENCY-DOMAIN DESIGN TECHNIQUE FILTERS	DFIR	(10 Hours)						
FIR And IIR Filter Specifications And Structure, FIR Filter Design- Window Method, Park- s Method, Frequency Sampling Method; Design Of IIR Digital Filters:Butterworth, Chebyshev And Elliptic Approximations. Low Pass, Band Pass, Band Stop And High Pass Filters, Bilinear Transformation Method, Adaptive Signal Processing								
EFFECT OF FINITE REGISTERS LENGTH					(05 Hours)			
Number Representation, Quantization Error, Round-Off Error, C Behavior, Noise Filtering By LSI System, Noise In A Cascade C				•				
MULTIRATE TECHNIQUES					(09 Hours)			
General Rate-Changing System, Integer-Factor Interpolation A Changing, Efficient Multirate Filter Structures, Optimal Filter Do Multirate Systems, Over sampling D/As, Perfect-Reconstruction	esign	For N	Aultira	ite Syste	ms, Multi-Stage			
APPLICATIONS OF DSP					(12 Hours)			
Speech And Radar Signal Processing; Signal Detection, Spectral Musical Sound Processing, Digital FM Stereo Generation, Speec Transmission Of Digital Data, Digital Audio Sampling Rate Co	ch Pr	ocessi	ng, D	iscrete N	Iulti-Tone			
			(Tota	al Conta	ct Time: 42 Hours)			
BOOKS RECOMMENDED:								
1. Salivahanapriya S,"Digital Signal Processing", Tata McGraw-	Hill,	2003						
2. Rabiner L. R. and Gold B., "Theory And Applications Of Digi	tal S	ignal	Proces	ssing", P	rentice Hall,1992			
3. Oppenheim A. V. and Schafer, "Discrete Time Signal Processing", Prentice Hall, 1989								
4. Proakis John G. and Manolakis D.G., "Digital Signal Processing: Principle, Algorithms And Applications", Prentice Hall, 1997								

5. Mitra Sanjit K., "Digital Signal Processing - A computer Based Approach", McGraw-Hill, 2005

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M. Tech. I (EC) [CS/VLSI] Semester I	L	T	P	C	
EC619:INFORMATION THEORY AND CODING(NEW)	3	0	0	3	
INFORMATION THEORY					(09 Hours)
Review Of Probability Theory, Introduction, Measure Of Informatic Symbols In Long Independent Sequences, Average Information Consequences, Properties Of Entropy, Extension Of Zero Memory Sciences	ntent	_			
SOURCE CODING					(07 Hours)
Properties Of Codes, Uniquely Decodable Codes, Kraft's Inequality First Theorem, Shannon's Encoding Algorithm, Shanon-Fano Code Code Efficiency And Redundancy		_	_		-
COMMUNICATION CHANNELS					(06 Hours)
Introduction, Discrete Communication Channels, Continuous Cha Equivocation, Mutual Information, Channel Capacity, Channel Effi Channels, Shannon-Hartley Law And Its Implications BLOCK CODES AND LINEAR CODES					
Single Parity Check Codes, Product Codes, Hamming Codes, Ham	ming	Code	s Mi	nimum	` ` '
Codes, Linear Block Codes, Generator Matrices, Parity Check Ma Detection, Minimum Distance, Error Correction And Error Detection Signal Constellations, Hard-Decision And Soft Decision Decoding	trices on Ca	, Enc	oder,	Synd	rome And Error
CYCLIC, BCH & CONVOLUTION CODES					(12 Hours)
Definition Of Cyclic Codes, Polynomials, Generator Polynomial, E Generator And Parity-Check Matrices Of Cyclic Codes, Linear Alg BCH Codes, Introduction To Convolution Codes, Introduction To	ebra 1	And (Galoi		
		(Tota	l Cont	act Time:42 Hours)
BOOKS RECOMMENDED					
1. Abrahamson N., "Information Theory and coding", McGraw-Hill					
2. Ranjan Bose, "Information theory, coding and cryptography", Tat	a Mc	Graw-	-Hill	,2nd E	dition,2008
3. Salvatore Gravano, "Introduction to Error Control Codes", Oxford	l Univ	ersity	y Pre	ss,1st	Edition,2007

4. Proakis J.J., "Digital Communications", McGraw Hill, 2nd Edition, 1989 5. Todd K.Moon, "Error Correcting Coding", Wiley India Edition, 2006



M. Tech. I (EC) [VLSI/CS] Semester I	L	Т	P	C	
EC617:VLSI TECHNOLOGY(NEW)	3	0	0	3	
ENVIRONMENT FOR VLSI TECHNOLOGY					(03 Hours)
Clean Room And Safety Requirements, Wafer Cleaning Processes A	And W	/et C	hem	ical E	tching Techniques
IMPURITY INCORPORATION					(05 Hours)
Solid State Diffusion Modeling And Technology, Ion Implantation I Annealing, Characterization Of Impurity Profiles	Model	ing,	Tecl	nolog	y And Damage
OXIDATION					(08 Hours)
Kinetics of Silicon Dioxide Growth Both for Thick, Thin And Ultra VLSI And ULSI, Characterization Of Oxide Films, High K And Lo					U
LITHOGRAPHY					(04 Hours)
Photolithography, E-Beam Lithography And Newer Lithography Te Generation	chniq	ues I	For V	/LSI/U	JLSI, Mask
CHEMICAL VAPOUR DEPOSITION TECHNIQUES					(07 Hours)
CVD Techniques For Deposition Of Polysilicon, Silicon Dioxide, S. Epitaxial Growth Of Silicon, Modeling And Technology	ilicon	Nitr	ide A	And M	etal Films,
METAL FILM DEPOSITION					(05 Hours)
Evaporation And Sputtering Techniques, Failure Mechanisms In Me Metallization Schemes	etal In	terco	onne	ets, M	ulti-Level
PLASMA AND RAPID THERMAL PROCESSING					(06 Hours)
PECVD, Plasma Etching And RIE Techniques, RTP Techniques Fo Various Films For Use In ULSI	r Ann	ealin	ıg, G	rowth	And Deposition Of
PROCESS INTEGRATION					(04 Hours)
NMOS, CMOS And Bipolar Circuits, Advanced MOS Technologies	S				
		('.	Γota	l Cont	tact Time:42 Hours)
BOOKS RECOMMENDED					
1. Chang C.Y. and Sze S. M., "VLSI Technology", McGraw Hill, 199	6				
2. Ghandhi S. K., "VLSI Fabrication Principles", John Wiley Inc., Ne	w Yor	k,19	83		
3. Sze S. M., "VLSI Technology", McGraw Hill, 2nd Edition, 1988					
4. Stephen A. Campbell,"The Science & Engineering of Microelect Press,2nd Edition,2001	ronics	Fab	ricat	ion", (Oxford University
5. Peter Van Zant, "Microchip Fabrication: A Practical Guide To Ser Hill,4th Edition,2000	micon	duct	or Pı	ocessi	ng", McGraw-



M. Tech. I (EC) [VLSI] Semester I	L	T	P	C				
EC623:HARDWARE DISCRIPTION LANGUAGES(NEW)	3	0	0	3				
INTRODUCTION					(10 Hours)			
Basic Concepts Of Hardware Description Languages, Hierarchy, Ostructural, Data-Flow And Behavioral Styles Of Hardware Descripsimulators			•	_	•			
SYNTAX AND SEMANTICS OF VHDL					(14 Hours)			
Syntax And Semantics Of VHDL, Variable And Signal Types, Arrays And Attributes, Operators, Expressions And Signal Assignments, Entities, Architecture Specification And Configurations, Component Instantiation, Concurrent And Sequential Constructs, Use Of Procedures And Functions, Examples Of Design Using VHDL								
SYNTAX AND SEMANTICS OF VERILOG					(18 Hours)			
Syntax And Semantics Of Verilog, Variable Types, Arrays And T Assignments, Modules, Nets And Registers, Concurrent And Sequ Examples Of Design Using Verilog, Synthesis Of Logic From Har	ienti	al Coi	nstruc	ets, Task	•			
			(Tota	al Conta	act Time: 42 Hours)			
BOOKS RECOMMENDED:								
1. Perry D., "VHDL", Tata McGraw-Hill, 2nd Edition, 2000								
2. Bhaskar J., "VHDL Primer", Pearson Education Asia, 2001								
3. Navabi Z., "VHDL", McGraw Hill International Edition, 1998								
4. Palnitkar S., "Verilog HDL: A Guide to Digital Design and Synthesis", Prentice Hall NJ, USA, 1996								

5. Bhaskar J., "Verilog HDL Synthesis - A Practical Primer", Star Galaxy Publishing, Allentown, 2003



M. Tech. I (EC) [VLSI] Semester I	L	T	P	C		
EC625:DEVICE MODELLING AND SIMULATION(NEW)	3	0	0	3		
DEVICE PHYSICS						(05 Hours)
The P-N Junction, Review Of Semiconductor Physics, The Built I Capacitance, Diode Current /Voltage Characteristics, Minority C						Junction
BIPOLAR TRANSISTORS						(08 Hours)
Current Gain, Gummel Plots And Output Characteristics, Recomb Region, Charge Storage And Forward Transit Time, Cutoff Freque Eber's-Moll And Gummel-Poon Model, Parameter Extraction, T	ency,	TTL	Gate	es, Ba	sic SPICE I	
MOS TRANSISTORS						(10 Hours)
Threshold Voltage And Body Effect, Current / Voltage Characteri Width Effect, Drain Induced Barrier Lowering, Channel Length Mobility And Velocity Saturation, SPICE Models, MOS Inverte	Iodul	ation				
SPICE SIMULATION						(10 Hours)
Analysis Of Complex Electronic Circuits, Simulation And Analys Sensitivity, DC Sweep Transfer Function, Frequency Response, Response, Distortion And Spectral Analysis, Device Models, Sin Circuits And Systems.	Feed	back	Con	trol A	nalysis, Tra	ansient
PROCESS SIMULATION						(09 Hours)
Oxidation And Chemical Vapor Deposition, Lithography And Etc Alignment And Self Alignment, Isolation In MOS Processes, Elec Metallization, The Silicon Gate CMOS Process, CMOS Design La	ctron	Mig	ratior es, Pr	n And ocess	Multilevel Simulation	
			(Tota	al Cor	ntact Time:	42 Hours
BOOKS RECOMMENDED:						
1. Hodges D.A., Jacksonh.G.,"Analysis And Design Of Digital In International,2000	tegra	ted C	ircuit	ts",Mo	Graw-Hill	
2. Uyemura J. P.,"Introduction To VLSI Circuits And Systems",Jo	ohn V	Viley	And	Sons,	2004	
3. Taur Y. and Ning T.H. "Fundamentals of Modern VLSI Device	es, ",	Cam	bridg	e Uni	versity Pres	ss, 2004
4. Eshraghian K. and Weste N. H. E., "Principles Of CMOS VLSI Perspective", Addison Wesley 2000	Desi	ign –	A Sy	stems		

5. Sze S. M., "Physics Of Semiconductor Devices" John Willey, 2nd Edition, 1981



 \mathbf{C}

EC629:PROBABILITY AND RANDOM PROCESSES(NEW)	3	0	0	3	
INTRODUCTION TO PROBABILITY THEORY					(05 Hour
Sets, fields, sample space and events, axiomatic definition of probab conditional probabilities, Independence, total probability, Bayes' re		Con	bina	torics,J	oint and
RANDOM VARIABLES					(12 Hour
Cumulative Distribution Function, Probability Density Function. For Probability Density, Joint Cumulative Distribution And Probability I moment generating functions, Average Value And Variance Of A R Density, Error Function, Rayleigh Probability Density, Mean And Variables, Correlation Between Random Variables, Central Limit Theorror and orthogonality principle, Chebysev inequality Sequences Of Sequences Of Random Variables. Weak law of large number.	Densi ando Varia neore	ity, C m Va ince (m, lii	harad riabl Of Therman	cteristic e, Gaus he Sum ninimur	e functions and ssian Probability of Random mean square
STOCHASTIC PROCESSES					(10 Hour
Stationary, Nonstationary, Strict-Sense and Wide-Sense Stationary Frocess and the Markov Process	roce	sses,	Gaus	ssian Pr	cocesses, Poisson
EXPECTED VALUES OF A RANDOM PROCESS					10 Hour
The Mean Value, Autocorrelation, Autocovariance, Power Spectral Two Random Processes, Crosscorrelation And Crosscovariance, Erg		ity, M	Iean	Square	•
Square Derivative And Mean Square Integral Of Stochastic Processes	es, Eı	godio	e Pro	cesses	
	es, Ei	godio	e Pro	cesses	(08 Hour
Square Derivative And Mean Square Integral Of Stochastic Processes					`

BOOKS RECOMMENDED

M. Tech. I (EC) [CS/VLSI] Semester I

- 1. Papoulis, "Probability, Random Variables And Stochastic Processes", McGraw-Hill,4th Ed., 10th Reprint,2006
- 2. Larson H. J. and Shubert B. O. "Probabilistic Models In Engineering Science Vol I, Random Variable And Stochastic Process, Vol II Random Noise Signals And Dynamic Systems", Wiley Publication, 1st Ed., 1982
- 3. Gardener W., "Stochastic Processes", McGraw-Hill,1st Ed.,1986
- 4. Montgomeri and Ruger, "Applied Statistics And Probability For Engineers", John Wiley, 1st Ed., 2006
- 5. Hayes Monson H., "Statistical Digital Signal Processing", John Wiley, 1st Ed., 1996
- 6. Alberto leon Gracia, Probability and Random processes for electrincal engineer,: 2nd Ed, PE india

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विभागीय प्रमुख: २२०१५५१, विभाग कार्यालय: २२०१५५२

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Appendix 1

Sr. No.	Course Name	Code	Teaching Scheme		0		U				U								Examina	Total
			L	T	P		Theory	Tutorial	Practical											
1	ANALOG VLSI DESIGN(NEW)	EC 612	3	0	0	3	100			100										
2	REAL TIME SYSTEMS(NEW)	EC 614	3	0	0	3	100			100										
3	VLSI LAB - II(NEW)	EC 616	0	0	8	4			100	100										
4	Elective III	EC 6XX	3	0	0	3	100			100										
5	Elective IV	EC 6XX	3	0	0	3	100			100										
6	Elective V	EC 6XX	3	0	0	3	100			100										
Total	[l	15	0	8	19	500		100	600										

LIST OF SUBJECTS FOR ELECTIVE III, IV & V	
Image Processing	EC602
Wireless Communication	EC604
Reconfigurable Computing	EC618
Microwave Integrated Circuits [Pre-requisite:EC601]	EC632
Optical Signal Processing	EC634
Ad-Hoc Networks	EC636
Low Power VLSI Design	EC622
Nanoelectronics	EC624
DSP Structures for VLSI [Pre-requisite: EC605]	EC626
VLSI System Design [Pre-requisite:EC623]	EC642
Testing and Verification of VLSI Circuits [Pre-requisite:EC623]	EC644



Appendix 2

		_			1
M. Tech. I (EC) [VLSI/CS] Semester II	L	T	P	C	
EC612:ANALOG VLSI DESIGN(NEW)	3	0	0	3	
ANALOG CMOS SUB-CIRCUITS					(09 Hours)
Small Signal Model For MOS, MOS Switch, MOS Resistors, Curre Current Mirrors, Differential, Cascode And Current Amplifiers Outparchitectures					
CMOS OPERATIONAL AMPLIFIERS					(09 Hours)
Design Of CMOS Operational Amplifiers, Compensation, Compara Cascode Op-Amps, Simulation And Measurement Techniques	tors,	Desi	gn O	f Two	Stage Op-Amps,
HIGH PERFORMACE CMOS OP-AMPS					(06 Hours)
Buffered Op-Amps, High Speed/Frequency Op-Amps, Differential Amps, Low Noise And Low Voltage Op-Amps	Outp	ut O _l	p-An	nps, M	icro Power Op-
SWITCHED CAPACITOR FILTERS					(09 Hours)
Switched Capacitor Circuits: Design And Analysis, Switched Capacitor Integrators, Z Domain Models, 1st And 2nd Order Switch Capacito		_			_
D/A AND A/D CONVERTERS					(09 Hours)
Sample And Hold Circuits. Characterization Of DAC, Nyquist Rate Parallel DAC, Serial DAC, Characterization Of ADC, Serial ADC, Techniques					
		(7.	Fota l	l Cont	act Time: 42 Hours)
BOOKS RECOMMENDED:					
1. John D.A. and Martin K., "Analog Integrated Circuit Design", Wil	ey,19	997			
2. Razavi Behzad, "Design of Analog CMOS Integrated Circuit", Tat	а М	cGrav	w-Hi	11,2002	2
3. Allen Philip and Holberg Douglas, "CMOS Analog Circuit Design	n",O	xford	Uni	versity	Press,2002
4. Gregorian R. and Temes G.C.," Analog MOS ICs for Signal Proce	essin	g", W	Viley	1986	
5. Baker Jacob R., Harry W. Li and Boyce David E., "CMOS: Circu	it De	esign,	Lay	out an	d Simulation", Wiley

Interscience, 2003



M. Tech. I (EC) [VLSI/CS] Semester II	L	T	P	C	
EC614:REAL TIME SYSTEMS(NEW)	3	0	0	3	
INTRODUCTION TO REAL TIME SYSTEMS					(10 Hours)
Hard Versus Soft Real Time Systems, Reference Models Services, I/O Subsystems, Network Operations Systems, Systems Interrupt Routines In RTOS Environments, RTO Latency And Response Time, Standardization Of RTO	Rea S Ta	al Ti	me I	Embedded	Systems, Operating
REAL-TIME SCHEDULING AND SCHEDULABIL	ITY	AN	AL'	YSIS	(09 Hours)
Task, Process And Threads, Commonly Used Approach Scheduling, Priority Driven Scheduling Of Periodic Taschedules, Earliest Dead Line First (EDF) Scheduling, Embedded Operating Systems: Standard & Perspective, Resource Management Aspects, Quasi-Static Determining	sks, late Real g Bo	Hyl Mon l Tin ound	orid itori ne O s On	Schedules ng Alog (I perating S Execution	, Event Driven RMA), Real Time ystems: Scheduling
INTER-PROCESS COMMUNICATION AND SYNC PROCESSES, TASKS AND THREADS	HK	ONI.	LA I	IONOF	(05 Hours)
Multiple Process in An Application, Data Sharing By M Communication	ultip	ole T	asks	And Rout	ines Inter Process
REAL TIME OPERATING SYSTEMS					(09 Hours)
Handling Resources Sharing and Dependencies Among Among real Time tasks, Priority Inversion, Priority Inh Protocol (HLP), Priority Ceiling Protocol (PCP), Differe Important Features of PCP, Handling Task Dependencie	erita nt T	ince	Prot	ocol (PIP)	, Highest Locker
COMMERCIAL REAL TIME OPERATING SYSTI	EMS	5			(09 Hours)
Time Services, Unix As Real Time OS, Non-Primitive Based Real Time OS, Extension to the Traditional Unix Point Approach, RT Linux, Windows CE As Real Time	Ker	nal,	Host	Target A	pproach, Preemption
			(Te	otal Conta	nct Time: 42 Hours)
BOOKS RECOMMENDED:					
1. Rajib Mall, "Real Time Systems Theory And Practice	",Pe	arsoı	n Ed	ucation,20	07
2. Wayne Wolf, "Computers as Components: Principles Design", Morgan Kaufman, 2001	of E	mbe	dded	Computin	g System
3. Liu Jane, "Real-time Systems", PHI, 2000					
4. Laplante Phillip A,"Real-Time Systems Design and A	naly	sis:	An]	Engineer's	Handbook",2005
5. Albert M. K. Cheng, "REAL-TIME SYSTEMS ScheolInterscience,2002	dulir	ng, A	naly	sis, and V	erification",Wiley
6. Richard Zurawski, "Embedded Systems Handbook",C	RC	Tay	lor F	rancis,200	6



M. Tech. I (EC) [VLSI] Semester II	L	T	P	C	
EC616:VLSI LAB - II(NEW)	0	0	8	4	
1.Simulation Of Analog Sub Circuits					
•MOS Switch					
•Current Sink/Source					
•Current Mirror Circuit					
•Cascode Amplifier					
2. Design And Simulation Of OP-AMPS					
3. Design And Simulation Of A/D Converter Circuit					
4. Introduction Of RT Linux, MuC/OS-II					
5. Task Management, Inter Process Communication Using RT Linux	/Mu	OS-	II		
6. Parting Real Time OS On Target Hardware And Task Profiling					_
7. Device Driver					

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LIST OF SUBJECTS FOR ELECTIVE III, IV & V

M. Tech. I (EC) [CS/VLSI] Semester II	L	T	P	C			
EC602:IMAGE PROCESSING(NEW)	3	0	0	3			
IMAGING SYSTEM					(04 Hours)		
Camera Model, Image Representation, Human Visual Perception And	Col	or, I	ligh-	Dynaı	mic-Range Imaging		
IMAGE ANALYSIS					(08 Hours)		
Spatial Filters, 2D Convolution, Discrete Fourier Transform, DCT, W. Concept Of Filtering, Smoothing And Sharpening, Edge Detection	alsh	Tran	sfori	n, KL	T And DWT,		
LOW-LEVEL IMAGE PROCESSING					(15 Hours)		
Point Operators, Histogram Processing, Image Restoration, Image Enh Morphological Processing, Image Segmentation	nanc	emer	nt, In	nage C	Compression,		
HIGH-LEVEL IMAGE PROCESSING					(07 Hours)		
Image Representation, Hough Transform For Feature Extraction, Shap Texture Description, Object Recognition And Tracking	e Ex	ktracı	tion,	Bound	dary Description,		
ADVANCED PHOTOGRAPHY					(08 Hours)		
Introduction To Image Cloning, Warping, Morphing, Imprinting, Wat Image Rendering	erma	arkin	g, Sı	iper R	esolution Image,		
		(To	otal (Conta	ct Time: 42 Hours)		
BOOKS RECOMMENDED:							
1. Gonzalez Rafel C. and Woods Richard C., "Digital Image Processing of India, 2nd Edition, 2002	g", I	Pears	on E	ducati	on, Prentice Hall		
2. Jain A.K., "Fundamentals Of Digital Image Processing", Prentice Ha	all o	f Ind	ia, 1s	st Edit	ion,1989		
3. Jain R., Kasturi R. and Schunck B.G: "Machine Vision", McGraw-H	Iill 2	2nd E	Editic	n,199	5		
4. Pratt W. K,"Digital Image Processing", Prentice Hall, 1st Edition,19	989						
5. Rosenfold and Kak A.C,"Digital Image Processing", Vol. 1 and 2, F	Prent	ice I	Hall,	1st Ed	lition,1986		
6. Milan Sonka, Vaclav Hlavac and Roger Boyle, "Image processing, Analysis, And machine Design", Thomson Publishing, India, 2nd Edition, 2007							

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M. Tech. I (EC) [CS/VLSI] Semester II	L	T	P	C	
EC604:WIRELESS COMMUNICATION(NEW)	3	0	0	3	
GENERAL CONSIDERATIONS					(12 Hours)

General Considerations About Radio Waves Over Wireless Channel, Radio Propagation And The Atmosphere, Basic Propagation Mechanisms In General, Radio Propagation Categories For Long Distance Case, Short Distance NLOS Mobile Communication Case, AWGN Model Showing Reflection, Scattering And Diffraction Of Radio Waves For Mobile Systems/Multipath Effect, Large Scale Fading, Small Scale Fading, Delay Spread Effect, ISI, Doppler Shift/Spread, Doppler Power Spectrum, Flat And Frequency Selective Fading

CHANNEL MODELS (05 Hours)

Channel Models, Equalization Techniques And Diversity Techniques

SPREAD SPECTRUM MODULATION

(13 Hours)

Basic Principle Of Orthogonality, Subcarrier Setting In The Spectrum, FDM Vs Orthogonal FDM, OFDM Block Diagram And Explanation, Pulse Shaping And Windowing In OFDM, Synchronization In OFDM, Pilot Insertion In OFDM Transmission And Channel Estimation, Amplitude Limitations, FFT Points Selection Constraints, CDMA Vs OFDM, Hybrid OFDM, MIMO

OFDM (13 Hours)

Spread Spectrum Modulation Concepts, ML, Walsh-Hadamard, Gold Sequences, Code Properties, Auto And Cross Correlation, Partial Correlation, DSSS Transmitter, Rake Receiver Block Diagram, PN Signal Characteristics, Spectral Density, Bandwidth And Processing Gain, Interference Rejection, Antijam Characteristics, Energy And Bandwidth Efficiency, Near Far Problem And Power Control, Frequency Hopping Spread Spectrum, Time Hopping, Comparison Of Spread Spectrum Modulation Methods, Hybrid Spread Spectrum System, Chirp Spread Spectrum

(Total Contact Time: 42 Hours)

BOOKS RECOMMENDED:

- 1. Upena Dalal, "Wireless Communication", Oxford University Press, 1st Edition, 2008
- 2. Molisch Andreas F., "Wideband Wireless Digital Communication", Pearson Education, 3rd Indian Reprint, 2003
- 3. Sharma Sanjay, "Wireless Communications", Katsons Books, 2006
- 4. Rappaport, T. "Wireless Communications", Pearson Education, 5th Indian Reprint, 2003
- 5. Schulze Henrik and Luders Christian, "Theory And Applications Of OFDM And CDMA Wideband Wireless Communications", Wiley, 2005
- 6. Goldsmith Andrea, "Wireless Communications", Cambridge University Press, 2002
- 7. Feher Kemilo, "Wireless Digital Communication", PHI, 1995

फ़ोन नं: संस्थान कार्यालय: २२२३३७१-७४, फैक्स नं: २२२८३९४,२२२७३३४

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M. Tech. I (EC) [CS / VLSI] Semester II	L	T	P	C	
EC618:Reconfigurable Computing(NEW)	3	0	0	3	
INTRODUCTION					(06 Hours)
General overview, Goals and motivations, History, state of the articles of study, Performance, power, and other metrics, Algorithm tutorial, RC Architectures, Device characteristics, Fine-grained at	m analy	sis a	nd sp	eedup	projections, VHDL
FPGA Physical Design Tools					(08 Hours)
Technology mapping, Placement & routing, Register Transfer (R) synthesis, Logic minimization	Γ)/Logi	e Syr	thesi	s, Con	troller/Datapath
RC Application Design					(10 Hours)
Parallelism, Systolic arrays, Pipelining, Optimizations, Bottlened High-level languages, Design tools	cks, Hig	gh-le	vel D	esign,l	High-level synthesis,
System architectures:					(10 Hours)
Hybrid architectures, Communication, Hw/sw partitioning, Soft strategies, System services, Small-scale architectures, HPC arch synthesis, Architectural design space explorations.					ctures, System
Case Studies & Special Topics:					(08 Hours)
Signal and image processing, Bioinformatics, Security, Partial R Performance Analysis/Prediction, Fault Tolerance	econfig	urati	on, N	lumeri	cal Analysis,
		(Tota	l Cont	act Time: 42 Hours)
BOOKS RECOMMENDED:					
1. C. Maxfield, "The Design Warrior's Guide to FPGAs", Newnes	,2004				
2. M. Gokhale and P. Graham, "Reconfigurable Computing: According Programmable Gate Arrays", Springer, 2005	eleratin	g Co	mput	ation v	vith Field-
3. C. Bobda, "Introduction to Reconfigurable Computing: Archite Applications", Springer, 2007	ectures,	Algo	orithr	ns and	
4. P. Lysaght and W. Rosenstiel (eds.), "New Algorithms, Archite Computing", Springer, 2005	ectures	and	Appl	ication	s for Reconfigurable
5. D. Pellerin and S. Thibault, "Practical FPGA Programming in	C" Pre	ntice	-Hall	,2005	
6. W. Wolf, "FPGA-based System Design", Prentice-Hall, 2004					
7. R. Cofer and B. Harding, "Rapid System Prototyping with FPC Process", Newnes, 2005	GAs: A	ccele	rating	g the D	esign
8. N. Voros and K. Masselos (eds.), "System-Level Design of Re Chip", Springer, 2005	configu	rable	Sys	tems-o	n-

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9. G. De Micheli, "Synthesis and Optimization of Digital Circuits", McGraw-Hill, 1994



M. Tech. I (EC) [CS/VLSI] Semester II	L	T	P	C					
EC632:MICROWAVE INTEGRATED CIRCUITS(NEW)	3	0	0	3					
ACTIVE RF COMPONENTS	(12 Hours)								
RF Diodes, Bipolar-Junction Transistor, RF FET									
ACTIVE RF COMPONENT MODELING	(10 Hours)								
Diode Models, Transistor Models, Measurement Of Active Devices, Characterization	Scat	tering	g Par	amete	r Device				
RF TRANSISTOR AMPLIFIER DESIGNS					(10 Hours)				
Characteristics Of Amplifiers, Amplifier Power Relations, Stability Considerations, Constant Gain, Noise Figure Circles, Constant VSWR Circles, Broadband, High-Power And Multistage Amplifiers									
OSCILLATORS AND MIXERS					(10 Hours)				
Basic Oscillator Model, HF Oscillator Configuration, Basic Characte	ristic	s Of	Mix	ers					
		(T	otal	Conta	act Time: 42 Hours)				
BOOKS RECOMMENDED:									
1. Ludwig Reinhold and Bretchko Pavel, "RF Circuit Design: Theory Education, 3rd Indian Reprint, 2004	And	l App	olicat	tions",	Pearson				
2. Massobrio G. and Antognetti P., "Semiconductor Device Modelling	g Wi	th SI	PICE	",McC	6raw- Hill,1993				
3. Gonzalez G., "Microwave Transistor Amplifiers- Analysis And De	sign'	",Pre	ntice	Hall,1	1997				
4. Gentili Christian, "Microwave Amplifiers And Oscillators", North Edition, 1986	Oxfo	ord A	cade	emic,R	evised				
5. Vendelin G., Pavio A and Rhode U. L., "Microwave Circuit Design Techniques", John Wiley, 1990	ı Usi	ng L	inea	r And]	Nonlinear				



M. Tech. I (EC) [CS/VLSI] Semester II	L	T	P	C				
EC634:OPTICAL SIGNAL PROCESSING(NEW)	3	0	0	3				
DIFFRACTION THEORY					(09 Hours)			
Huygen's Principle, Fraunhofer Diffraction, Fresnel Diffraction, Kirc Diffraction Waves, Diffraction Grating	hhof	f's D	iffra	ction '	Γheory, Boundary			
COHERENCY					(05 Hours)			
Interference, Visibility, Coherence Function, Spatial Coherence, Temp	oral	Coh	eren	ce				
FOURIER OPTICS					(08 Hours)			
Optical Fourier Transform, Linear System, Convolution, Correlation, Theory, Optical Transfer Function	Four	ier N	1etho	ods In	Diffraction			
INFORMATION OPTICS					(08 Hours)			
Spatial Frequencies, Abbe's Theory, Spatial Filtering, Phase Contrast, Filters, Spatial Light Modulator	Ima	ging	Enh	ancem	ent, Optical			
APPLICATION OF OPTICAL SIGNAL PROCESSING					(06 Hours)			
Holography, Information Processing, Optical Pattern Recognition								
ADVANCED OPTICAL SIGNAL PROCESSING					(06 Hours)			
Digital Optics, Optical Computing, Optical Neural Network								
		(Te	otal	Conta	ct Time: 42 Hours)			
BOOKS RECOMMENDED:								
1. Goodman J., "Introduction to Fourier Optics", McGraw Hill, 2nd Ed	litio	n,200	00					
2. Hecht E., "Optics", Addison Wesley, 4th Edition, 2001								
3. Anthony Vanderlugt, "Optical Signal Processing", John Wiley & So	ns,2	005						
4. Okan K. Ersoy, "Diffraction, Fourier Optics and Imaging", Wiley-In	4. Okan K. Ersoy, "Diffraction, Fourier Optics and Imaging", Wiley-Inter Science, 2006							
5. W.T. Rhodes, "Fourier Optics and Optical Signal Processing", Wiley								



M. Tech. I (EC) [CS/VLSI] Semester II	L	T	P	C	
EC636:AD-HOC NETWORKS(NEW)	3	0	0	3	
INTRODUCTION					(04 Hours)
Introduction To Generations In Wireless Systems, Introduction Classification Of Mobile Data Networks	n To Mo	bile A	Ad-H	oc Netv	works (MANETS),
BLUETOOTH					(08 Hours)
Bluetooth Network Structure: Piconet & Scatternet, Bluetooth Bluetooth Media Access Control Consideration, Asynchrone Connection Oriented Communication Link, Modified Blueto	ous Conne				
WIFI - IEEE802.11 STANDARDS					(08 Hours)
Various 802.11 Protocols (a to s), WiFi Architecture, Security MAC Layer Aspects Of 802.11 a,b,g,e,n; WiFi MAC: Point Contion, Hybrid Coordinate Function					
WiMAX - IEEE802.16 STANDARDS					(08 Hours)
Various 802.16 (a to e) Protocols, WiMAX Air Interface / Ph Protocol Architecture, WiMAX And WiFi Interworking, WiM	•				-
WIRELESS SENSOR NETWORK					(07 Hours)
Zigbee IEEE 802.15.4, Mobile Computing Aspects					
UWB					(02 Hours)
UWB Air Interface					
IEEE802.20 AND BEYOND					(02 Hours)
LONG TERM EVOLUTION					(03 Hours)
			(Tota	al Con	tact Time: 42 Hours)
BOOKS RECOMMENDED:					
1. Toh C. K., "Ad-hoc Mobile Wireless Networks", LPE, Pears	son Educa	ition,	2nd E	Edition,	2009
2. William C.Y. Lee, "Wireless & Cellular Telecommunication	n", McGr	aw-H	[i11,3r	d Editi	on,2005
3. Upena Dalal, "Wireless Communication", Oxford University	y,1st Edit	ion,2	009		
4. Vijay K. Garg, "Wireless Network Evolution 2G to 3G", Pe	arson Edu	catio	n,2nc	l Editic	on,2004
5. T. G. Palanievelu, R. Nakkeeran, "Wireless & Mobile Com	municatio	n",P	HI,1s	t Editio	on,2009
6. Schiller Jochen, "Mobile Communications", Addison Wesl Reprint,2000	ey, LPE,	Pears	on E	ducatio	n,4th indian



M. Tech. I (EC) [VLSI/CS] Semester II	L	T	P	C	
EC622:LOW POWER VLSI DESIGN(NEW)	3	0	0	3	
INTRODUCTION					(09 Hours)
Low Power VLSI, Modeling And Sources Of Power Consumption, Levels	, Pow	ver E	stima	tion A	t Different Design
POWER OPTIMIZATION					(14 Hours)
Combinational Circuits And Sequential Circuits Voltage Scaling Ap Energy Recovery Techniques, Low Power SRAM Architectures	proac	ches,	Low	Energy	/ ComputingUsing
SOFTWARE DESIGN					(08 Hours)
Software Design For Low Power VLSI Design, Computer Aided D	esigr	1 Too	ols		
CASE STUDIES					(11 Hours)
Recent Trends in Low-Power Design for Mobile And Embedded A	applic	cation	1		
		(Tota	l Cont	act Time: 42 Hours)
BOOKS RECOMMENDED:>					
1. Roy Kaushik and Prasad Sharat,"Low-Power CMOS VLSI Design	gn",J	ohn V	Wiley	& Soi	ns Inc,2000
2. Chandrakasan Anantha P. and Brodersen Robert W., "Low Powe Academic, 1995	r Dig	gital (СМО	S Desi	gn",Kluwer
3. Yeap Gary K., "Practical Low Power Digital VLSI Design", Klu	wer A	Acade	emic,	1998	
4. Kiat-Seng Yeo and Kaushi Roy, "Low Voltage Low Power VLSI Edition, 2004	I Sub	syste	ms",	McGra	w- Hill, 1st
5. Kang S. M., "CMOS Digital Integrated Circuits", Tata McGraw F.	Hill, 3	Brd E	ditior	n,2003	



M. Tech. I (EC) [VLSI/CS] Semester II	L	Т	P	C	
EC624:NANOELECTRONICS(NEW)	3	0	0	3	
INTRODUCTION TO MINIATURIZATION AND NANOSCALE PH	YSI	CS		•	(02 Hours)
Scaling Laws In Mechanics, Electricity, Electromagnetism And Optics The Atomic Orbitals, Electromagnetic Waves, The Quantization Of Energy, Ato The Photoelectric Effect, Wave-Particle Duality, The Uncertainty Principle	mic	Spe	ctra	And	Discreetness,
INTRODUCTION TO NANOSTRUCTURES AND MEMS					(15 Hours)
Nanostructures Like Particles, Wires, Films, Layers And Coatings, Porous Materials And Molecules, Historical Background Of MEMS, Silicon Pressu Mechanical Systems, Micro-fabrication And Micromachining: Integrated Of Micromachining, Isotropic Etching And Anisotropic Etching, Wafer Bondin	ire S Circu	Senso uit P	ors, i	Micro	-Electro- Bulk
APPLICATONS AREAS					(15 Hours)
b) Nanoelectronics: Electrons In Solids, Fermi Energy, Density Of States I Behavior Of The Solids, Quantum Confinement, Tunneling, Single Electron Electronics c) Nanophotonics: Photonic Properties Of Nanomaterials, Near-Field Light, Crystals	n Ph	enor	nenc	on, M	olecular , Photonic
NANOELECTRONIC DEVICES AND SYSTEMS					(10 Hours)
Resonant Tunneling Diode, Quantum Cascade Laser, Single Electron Trans Sensors And Actuators, Physical Microsensors And Actuators, Their Princ Examples					
	(To	tal (Cont	act T	ime: 42 Hours
BOOKS RECOMMENDED:					
1. Rogers, Pennathur and Adams, "Nanotechnology: Understanding Small Sprancis Group, 2008	ystei	ms",	CRO	Pres	ss, Tayler And
2. Fahrner W. R. (Ed), "Nanotechnology And Nanoelectronics: Materials, D Techniques", Springer Publications, 2005	evic	es, I	Meas	urem	ent
3. Kumar Vijay, "Nanosilicon", Elsevier Ltd., 1st Edition, 2008					
4. Kohler and Fritzsche, "Nanotechnology: An Introduction To Nanostructur 1st Edition, 1st Reprint, 2004	ing	Tec	hniq	ues",	Wiley-VCH,

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5. Mahalik N. P., "Micromanufacturing and Nanotechnology", Springer, 2006



M. Tech. I (EC) [VLSI/CS] Semester II	L	T	P	C	
EC626:DSP STRUCTURES FOR VLSI(NEW)	3	0	0	3	
VLSI ARCHITECTURES					(09 Hours)
VLSI Architectures for DSP Algorithms, Data Flow Represent Retiming, Unfolding, Register Minimization Techniques, Sys		-	_		Parallel Processing,
ALGORITHMS					(11 Hours)
Algorithm For Fast Implementation Of Convolution, FIR, IIR A Word Length Effects	and Ad	aptiv	e Filt	ers, D	CT, Analysis Of Finite
LOW POWER DESIGN STRATEGIES					(11 Hours)
Architecture And Applications Of General Purpose Digital Sig Programming Of TMS 320c55x/ Black Finn High Performance TMS320C6x/ SHARC					
APPLICATION CASE STUDIES					(11 Hours)
Speech Coding, Image Compression, Vitterbi Decoding, Wirele	ss Con	nmun	icatio	n	
			(Tot	al Co	ntact Time: 42 Hours)
BOOKS RECOMMENDED:					
1. Wanhammar Lars, "DSP Integrated Circuits", Academic Pres	s,1999				
2. Kuo S. M. and Lee B. H., "Real-Time Digital Signal Process Experiments With The TMS320C55X", Wiley, 2001	ng: Im	plem	entati	ions, A	Applications &
3. Parhi K. K., "VLSI Digital Signal Processing Systems: Design	And I	mple	ment	ation"	John Wiley 1999
4. Parhi K. K. and Nishitani T., "DSP For Multimedia Systems"	, Marce	el De	kker,	1999	

5. Higgins Richard J., "DSP in VLSI", PHI, 1990



M. Tech. I (EC) [VLSI] Semester II	L	T	P	C	
EC642:VLSI SYSTEM DESIGN(NEW)	3	0	0	3	
INTERCONNECT					(13 Hours)

The Wire, Interconnect Parameter, Electrical And Spice Wire Model, RLC Parasitic, Signal Integrity And High Speed Behavior Of Interconnects, Ringing, Cross Talk And Ground Bounce, Layout Strategies At IC And Board Level For Local And Global Signals, Power Supply Decoupling, Advance Interconnect Techniques

DESIGNING OF SEQUENTIAL LOGIC CIRCUIT

(13 Hours)

Static And Dynamic Latches And Registers, Design And Optimization Of Pipelined Stages, Timing Issues In Digital Circuits, Handling Multiple Clock Domains, Synchronous And Asynchronous Design Styles, Interface Between Synchronous And Asynchronous Blocks, Set-Up And Hold Time Violation, Concept Of Meta-Stability

SYSTEM HARDWARE DECOMPOSITION

(10 Hours)

Data Path & Control Path, Register Transfer Level Description, Control Path Decomposition (Interfacing With FSM), Pitfalls of Decomposition, Control Flow And Data Flow Pipelines, Communication Between Subsystems, Control Dead Locks

MEMORY SUBSYSTEM DESIGN

(06 Hours)

Memory Architecture, Shared Memory Data Hazards And Consistency, Mutual Exclusion

(Total Contact Time: 42 Hours)

BOOKS RECOMMENDED:

- 1. Rabaey Jan M., "Digital Integrated Circuits (Design Perspective)", Prentice Hall of India, 2nd Edition, 2003
- 2. Smith M. J. S., "Application Specific Integrated Circuits", Addison Wesley, 1999
- 3. Dally W. J. and Poulton J. W., "Digital System Engineering", Cambridge University Press, 1998
- 4. Hall S. H., Hall G. W. and McCall J. A., "High Speed Digital System Design", John Wiley And Sons, 2000
- 5. Bakoglu, "Circuit Interconnect And Packaging For VLSI", Addision-Wesley, 1990
- 6. Weste N. H. E., David Harris and Banerjee A., "CMOS VLSI Design", Addison Wesley, 3rd Edition, 2004

फ़ोन नं: संस्थान कार्यालय: २२२३३७१-७४, फैक्स नं: २२२८३९४,२२२७३३४

विभागीय प्रमुख: २२०१५५१, विभाग कार्यालय: २२०१५५२

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M. Tech. I (EC) [VLSI] Semester I	L	T	P	С	
EC644:TESTING & VERIFICATION OF VLSI CIRCUITS(NEW)	3	0	0	3	
INTRODUCTION					(10 Hours)
Scope Of Testing And Verification In VLSI Design Process, Issues Chips, Embedded Cores And SOCs	In T	est A	and V	'erifica	ation Of Complex
VLSI TESTING FAULT MODELS					(12 Hours)
Fundamentals Of Automatic Test Pattern Generation, Design For T And Boundary Scan, System Testing and Test For SOC, Delay Fa		•		n Desi	gn, Test Interface
Mu TESTING OF LOGIC AND MEMORIES					(10 Hours)
Test Automation, Design Verification Techniques Based On Simula Approaches	ation	, Ana	lytic	al And	Formal
VERIFICATION					(10 Hours)
Functional Verification, Timing Verification, Formal Verification, B Model Checking, Hardware Emulation	asics	of E	quiva	lence	Checking And
		(Tota	l Cont	act Time: 42 Hours)
BOOKS RECOMMENDED:					
1. Bushnell M. and Agrawal V. D., "Essentials Of Electronic Testing Signal VLSI Circuits", Kluwer Academic Publishers, 2000	g Foi	Dig	ital, I	Memoi	ry And Mixed-
2. Abramovici M., Breuer M. A. and Friedman A. D., "Digital System Press, 1990	ems '	Testi	ng A	nd Tes	table Design",IEEE
3. Kropf T., "Introduction To Formal Hardware Verification", Sprir	nger '	Verla	ıg,200	00	
4. Rashinkar P., Paterson and Singh L., "System-On-A-Chip Verific Techniques", Kluwer Academic Publishers, 2001	atior	n-Met	thodo	ology A	and
5. Neil H. E. Weste and David Harris, "Principles Of CMOS VLSI	Desig	gn",A	ddis	on Wes	sley, 3rd

Edition,2004



Appendix 1

	Course Name	Code		ching eme		Credit	Examina	Total		
			L	T	P		Theory	Tutorial	Practical	1
1	Dissertation Preliminaries	EC 805	0	0	16	8	0	0	400	400
2	Seminar	EC 807	0	0	4	2	0	0	100	100
Total		l	0	0	20	10	0	0	500	500



Appendix 1

	M.Tech.	II(EC), I	V Ser	nester	(VLS	I & Embed	lded Syster	ms)		
Sr. No.	Course Name	Code		ching eme		Credit	Examinat		Total	
			L	T	P		Theory	Tutorial	Practical	
1	Dissertation	EC 804	0	0	24	12	0	0	400	400
Tota	1	ı	0	0	24	12	0	0	400	400
Tota	l Contact Hour	s per week	: 24	•	•					